CLAIMS:

1. An integrated circuit comprising a processor (1), a data memory (2) and function blocks (4,5), in which a data bus (3) is provided for communication between the processor (1), the data memory (2) and the functional blocks (4,5), a logical direct connection on the data bus for a transfer of data between at least two function blocks (4, 5) being provided via a handshake method, with one function block (4) acting as master and one function block (5) acting as a slave, the latter having a linear address space to which the function block (4) acting as master can have access by way of the handshake method and which address space in the function block (5) acting as a slave is mapped onto a buffer memory.

2. An integrated circuit as claimed in Claim 1, characterized in that, the data bus (6), on which the handshake method takes place, is a standard bus system that is standardized for on-chip bus systems.

3. An integrated circuit as per Claim 1, characterized in that, the buffer memory is a ping-pong buffer (11), onto which the address space is cyclically mapped.

4. An integrated circuit as claimed in Claim 1 or 2, characterized in that, in the handshake method the function block (5) acting as a slave, sends an acknowledge message (13) to the function block (4) acting as master, after each permitted and finalized access of the function block acting as master to the linear address ranges.

5. An integrated circuit as claimed in Claim 1 or 2, characterized in that, in the handshake method the function block (5) acting as a slave sends an abort-try again acknowledge message (15) to the function block (4) acting as master after each rejected access of the function block (4) acting as master to the linear address ranges.

6. An integrated circuit as claimed in Claim 1, characterized in that, in the function block (4) acting as master is a JPEG-CODEC and the function block (5) acting as a slave is a memory interface which access an externally provided storage medium.